REMARKS

Applicant thanks the Examiner for examination of the application and the allowance of claims 7-14.

Claims 3 and 6 have been canceled. The limitations from Claims 3 and 6 have been added to the independent claims of which each depends from, Claims 1 and 4, respectively. Since Examiner ahs concluded that Claims 3 and 6 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, Claims 1, 2, 4 and 5 are allowable because they include the limitations from Claims 3 and 6, respectively.

The Examiner is requested to withdraw the rejection of claim 1, 2, 4 and 5 under 35 U.S.C. § 102(b) as anticipated by Lane U.S. Patent No. 5,648,923.

Amended Claim 1 recites:

A finite impulse response filter cell, having at least three inputs and at least two outputs, the finite impulse response filter cell coupled to receive a clocking signal, comprising:

a multiplexer having at least two multiplexer inputs and an output, the multiplexer operable at substantially half the clocking signal rate, each of the at least two multiplexer inputs coupled to one of the at least three inputs of the finite impulse response filter cell;

a multiplier including an output and at least two multiplier inputs, the first multiplier input receiving a coefficient signal representing a FIR coefficient, the

second multiplier input coupled to one of the at least three inputs of the finite impulse response filter cell;

a summer having at least two summer inputs and an output, the first and second summer inputs coupled to receive the multiplexer output and the multiplier output;

at least two slave sample and hold circuits each having a slave input and a slave output, the at least two slave inputs of the plurality coupled to the summer output, the at least two slave outputs couple to form the at least two outputs of the finite impulse response filter cell, each slave sample and hold circuit operable at substantially half the clocking signal rate; and

a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

Lane et al. teaches a multiplexer (408), a multiplier (402), a summer (410), and two slave sample and hold circuits (404, 406).

Amended claim 1 requires conversion circuitry.

Since the Lane et al. patent does not show nor suggest the claimed feature of amended Claim 1, Claim 1 is unanticipated and unobvious over Lane et al. as recited by Examiner.

Dependent claim 2 is also allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. Claim 2 at least provides claim differentiation.

Amended Claim 4 recites:

A finite impulse response filter cell, having at least two inputs and an output, the finite impulse response filter cell coupled to receive a clocking signal, comprising:

a multiplier including an output and at least two multiplier inputs, the first multiplier input receiving a coefficient signal representing a FIR coefficient, the second multiplier input coupled to one of the at least two inputs of the finite impulse response filter cell;

a summer having at least two summer inputs and an output, the first summer input coupled to receive the multiplier output, the second summer input coupled to one of the at least two inputs of the finite impulse response filter cell;

at least two slave sample and hold circuits each having a slave input and a slave output, the at least two slave inputs coupled to the summer output, each slave sample and hold circuit operable at half the clocking signal rate;

a multiplexer having at least two multiplexer inputs and an output, each of the at least two slave outputs coupled to one of the at least two multiplexer inputs, the multiplexer operable at half the clocking signal rate, the multiplexer output couples to form the output of the finite impulse response filter cell; and

a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

Lane et al. teaches a multiplexer (408), a multiplier (402), a summer (410), and two slave sample and hold circuits (404, 406).

Amended claim 4 requires conversion circuitry.

Since the Lane et al. patent does not show nor suggest the claimed feature of amended Claim 4, Claim 4 is unanticipated and unobvious over Lane et al. as recited by Examiner.

Dependent claim 5 is also allowable as depending on allowable independent amended Claim 4 and including further limitations that distinguish over the art. Claim 5 at least provides claim differentiation.

The Examiner is requested to withdraw the rejection of claim 1, 2, 4 and 5 under 35 U.S.C. § 102(e) as anticipated by Matsuura U.S. Patent No. 6,625,628.

Amended Claim 1 recites:

A finite impulse response filter cell, having at least three inputs and at least two outputs, the finite impulse response filter cell coupled to receive a clocking signal, comprising:

a multiplexer having at least two multiplexer inputs and an output, the multiplexer operable at substantially half the clocking signal rate, each of the at least two multiplexer inputs coupled to one of the at least three inputs of the finite impulse response filter cell;

a multiplier including an output and at least two multiplier inputs, the first multiplier input receiving a coefficient signal representing a FIR coefficient, the second multiplier input coupled to one of the at least three inputs of the finite impulse response filter cell;

a summer having at least two summer inputs and an output, the first and second summer inputs coupled to receive the multiplexer output and the multiplier output;

at least two slave sample and hold circuits each having a slave input and a slave output, the at least two slave inputs of the plurality coupled to the summer output, the at least two slave outputs couple to form the at least two outputs of the finite impulse response filter cell, each slave sample and hold circuit operable at substantially half the clocking signal rate; and

a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

Matsuura teaches a multiplexer (4), a multiplier (2), a summer (4), and two slave sample and hold circuits (25,35).

Amended claim 1 requires conversion circuitry.

Since the Lane et al. patent does not show nor suggest the claimed feature of amended Claim 1, Claim 1 is unanticipated and unobvious over Lane et al. as recited by Examiner.

Dependent claim 2 is also allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. Claim 2 at least provides claim differentiation.

Amended Claim 4 recites:

A finite impulse response filter cell, having at least two inputs and an output, the finite impulse response filter cell coupled to receive a clocking signal, comprising:

a multiplier including an output and at least two multiplier inputs, the first multiplier input receiving a coefficient signal representing a FIR coefficient, the

second multiplier input coupled to one of the at least two inputs of the finite impulse response filter cell;

a summer having at least two summer inputs and an output, the first summer input coupled to receive the multiplier output, the second summer input coupled to one of the at least two inputs of the finite impulse response filter cell;

at least two slave sample and hold circuits each having a slave input and a slave output, the at least two slave inputs coupled to the summer output, each slave sample and hold circuit operable at half the clocking signal rate;

a multiplexer having at least two multiplexer inputs and an output, each of the at least two slave outputs coupled to one of the at least two multiplexer inputs, the multiplexer operable at half the clocking signal rate, the multiplexer output couples to form the output of the finite impulse response filter cell; and

a conversion circuitry coupled to the second multiplier input, the conversion circuitry operable to convert a digital value at the second multiplier input into an analog signal.

Matsuura teaches a multiplexer (4), a multiplier (2), a summer (4), and two slave sample and hold circuits (25,35).

Amended claim 4 requires conversion circuitry.

Since the Lane et al. patent does not show nor suggest the claimed feature of amended Claim 4, Claim 4 is unanticipated and unobvious over Lane et al. as recited by Examiner.

Dependent claim 5 is also allowable as depending on allowable independent amended Claim 4 and including further

limitations that distinguish over the art. Claim 5 at least provides claim differentiation.

Claims 1, 2, 4, 5, and 7-14 stand allowable.

This Amendment, submitted in response to the outstanding office action dated March 31, 2004, is believed fully responsive to each point of objection or rejection raised therein.

The Claims 1, 2, 4, 5, and 7-14 distinguish over the cited references and the application is in allowable form. Applicant respectfully requests reconsideration or further examination and allowance of the application.

Respectfully submitted,

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